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Our Docket No.: CC-084/CPA / 1496.00251

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Applicant:	Alain P. Levesque		
Application No.:	09/390,090	Examiner:	Rouvas, N.
Filed:	September 3, 1999	Art Group:	2614
For:	TIME-SHIFTED VIDEO SIGNAL PROCESSING		

I hereby certify that this letter, the response or amendment attached hereto are being deposited with the United States Postal Service as first class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on June 20, 2003.

By: Mary Donna Berkley
Mary Donna Berkley

APPEAL BRIEF

Mail Stop - Appeal Brief Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Appellants submit, in triplicate, the following Appeal Brief pursuant to 37 C.F.R. §1.192 for consideration by the Board of Patent Appeals and Interferences. Please charge $320.00 to cover the cost of filing the opening brief as required by 37 C.F.R. §1.17(f) and any additional fees or credit any overpayment to Deposit Account Number 12-2252.

06/25/2003 DTESSEM1 00000077 122252 09390090
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I. REAL PARTY IN INTEREST

The real party in interest is the Assignee, LSI Logic Corporation.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences known to the Appellant, Appellant's legal representative, or Assignee which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-11 and 13-24 are pending and remain rejected. The Appellant hereby appeals the rejection of claims 1-11 and 13-24.

IV. STATUS OF AMENDMENTS

Appellant is appealing a final Office Action issued by the Examiner on December 31, 2002. On February 28, 2003, Appellant filed an Amendment After Final that amended the independent claims. On April 7, 2003, the Examiner issued and Advisory (i) indicating that the amendments raised new issues and thus would not be entered, (ii) indicating that the amendments would not be entered for the purpose of an appeal, and (iii) providing rational why the amendments would be rejected. On May 20, 2003, Appellant filed a Continued Prosecution Application with a preliminary amendment entering the amendments from the February 28, 2003 Amendment After Final. On May 20, 2003, Appellant also filed a Notice of Appeal.

V. SUMMARY OF INVENTION

The present invention concerns a time-shifted video method. The method generally comprises, (A) in a real-time mode, delivering real-time video frames for display in response to a digital input signal (201), (B) in a time-shifted mode, delivering time-shifted video frames for display in response to the digital input signal, the time-shifted video frames being delayed relative to the real-time video frames (213), and (C) pausing a real-time frame during a transition from the real-time mode to the time-shifted mode (205).

VI. ISSUES

The first issue is whether claims 1-5 and 23 are patentable under 35 U.S.C. §102(b) over Yifrach, U.S. Patent No. 5,329,320.

The second issue is whether claims 6-10, 13-22 and 24 are patentable under 35 U.S.C. §103(a) over Yifrach.

The third issues is whether claim 11 is patentable under 35 U.S.C. §103(a) over Yifrach in view of Russo et al., U.S. Patent No. 5,701,383.

VII. GROUPING OF CLAIMS

Appellant contends that the claims of the present invention do not stand or fall together. In particular, the following groups of claims are separately patentable:

Group 1: Claims 1 and 3-10 stand together.

Group 2: Claims 2 and 24 stand together.

Group 3: Claims 23, 15, 18 and 19 stand together.

Group 4: Claim 20 stands alone.

Group 5: Claims 21, 16 and 17 stand together.

Group 6: Claims 22, 13 and 14 stand together.

Group 7: Claim 11 stands alone.

The claim(s) in each group is(are) separately patentable from the claim(s) in any other groups.

VIII. ARGUMENTS

A. Selected groupings of claims are each patentable over Yifrach

35 U.S.C. § 102

The Federal Circuit has stated that "[t]o anticipate, *every element and limitation* of the claimed invention must be found in a single prior art reference, *arranged as in the claim.*"[1] (Emphasis added). The Federal circuit has added that the anticipation determination is viewed from one of ordinary skill in the art: "There must be no difference between the claimed invention and the reference disclosure, as viewed by a person of ordinary skill in the field of the invention."[2]

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[1] *Brown v. 3M*, 60 USPQ2d 1375, 1376 (Fed. Cir. 2001) citing *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1383, 58 USPQ2d 1286, 1291 (Fed. Cir. 2001); *Scripps Clinic & Research Found. v. Genentech Inc.*, 927 F.2d 1565, 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991) (Emphasis added by Appellant).

[2] *Scripps Clinic & Research Found. v. Genentech Inc.*, 927 F.2d 1565, 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991).

1. **Group 1 (claims 1 and 3-10) is fully patentable over Yifrach**

Claim 1 provides (i) pausing a real-time frame during a transition from a real-time mode to a time-shifted mode and (ii) delivering time-shifted video frames for display in a time-shifted mode. The Examiner has asserted that a normal viewing mode of Yifrach discloses the claimed real-time mode and a playback mode of Yifrach discloses the claimed time-shifted mode.[3] The text of Yifrach cited by the Examiner for the transition states:

> (c) Now whenever the viewer wishes to play back the 30 seconds of broadcast "frozen" by depressing the Freeze button 32, this is effected by depressing the Playback button 33, which controls the logic circuit 31 to select the Playback Mode.[4]

Nowhere in the above text or any other section does Yifrach disclose or suggest that real-time frames are **paused during a transition** from the real-time mode to the time-shifted mode as presently claimed. In contrast, Yifrach discloses that the "frozen" real-time frames used in the time-delay mode are **stored before a transition** from the real-time mode to the time-delay mode. In particular, Yifrach states:

> (b) When the Freeze button 32 is depressed, it controls the logic circuit 31 to select a Freeze Mode. In this mode, the cyclic storage device 23 is connected to the further storage device 30 to transfer its contents at that instant to the further storage device. That is, the last 30 seconds of the broadcast are thus "frozen" in the further storage device 30, while the cyclic storage device 23 continues to store the compressed audio and video signals last outputted by the compressor circuit 22 over the predetermined 30-second time interval.[5]

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[3] Advisory, April 7, 2003, page 2, lines 8-12.

[4] Yifrach, column 5, lines 12-16.

[5] Yifrach, column 4, line 64 to column 5, line 5.

Therefore, a transition from the normal viewing mode to the playback mode of Yifrach does not disclose or suggest pausing a real-time frame during a transition from a real-time mode to a time-shifted mode as presently claimed.

Assuming, *arguendo*, that a delayed viewing mode of Yifrach discloses the claimed time-shifted mode (for which the Appellant's representative does not necessarily agree), Yifrach is still silent regarding pausing a real-time frame during a transition between modes. Therefore, a transition from the normal viewing mode to the delayed viewing mode of Yifrach does not disclose or suggest pausing a real-time frame during a transition from a real-time mode and a time-delay mode as presently claimed.

Assuming, *arguendo*, that the freeze mode of Yifrach discloses the claimed time-shifted mode (for which the Appellant's representative does not necessarily agree), Yifrach is silent regarding delivering time-shifted video frames for display in a time-shifted mode as presently claimed. In particular, Yifrach states that a viewer "continues to see the broadcast in a real-time manner" when freezing frames in a RAM 30.[6] Contrary to the Examiner's assertion,[7] Yifrach appears to disclose that the initiation of the freeze mode and subsequent freezing of frames in the RAM 30 occurs **each time** a Freeze button 32 is pressed, not just after a second press.[8] Therefore, Yifrach does not disclose or suggest delivering time-shifted video frames for display in a time-shifted mode as presently claimed.

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[6] Yifrach, column 5, lines 10-11.

[7] Advisory, April 7, 2003, page 2, lines 8-11.

[8] Yifrach, column 4, line 64-column 5, line 11.

In summary, Yifrach does not disclose or suggest pausing a real-time frame during a transition from a real-time mode to a time-shifted mode as presently claimed. Yifrach also does not disclose or suggest delivering time-shifted video frames for display in a time-shifted mode as presently claimed. As such, the claimed invention is fully patentable over the cited reference and the rejection should be reversed.

2. Group 2 (claims 2 and 24) is fully patentable over Yifrach

The claims of group 2 depend from claim 1 and thus contain all of the limitations of claim 1. Consequently, the arguments presented above in support of the patentability of claim 1 (group 1) are incorporated hereunder in support of group 2.

Claim 2 further provides that the transition is between the paused real-time frame and a time-shifted version of the paused real-time frame. In contrast, Yifrach is silent regarding a "to" frame being a time-shifted version of a "from" frame regardless of the mode transition. The Examiner's assertion that frames presented from the cyclic storage device 23 and/or the RAM 30 of Yifrach are time-delayed frames is irrelevant since the claim involves a transition between specific frames during a mode transition. Nothing in Yifrach or the Examiner's arguments discloses that the first frame displayed from either the cyclic storage device 23 or the RAM 30 of Yifrach will be a time-shifted version of the last frame displayed from the real-time mode. Therefore Yifrach does not disclose or suggest a transition between a paused real-time frame and a time-shifted version of the paused real-time frame as presently claimed. As such, claims 2 and 24 are fully patentable over the cited reference and the rejection should be reversed.

3. Group 3 (claims 23, 15, 18 and 19) is fully patentable over Yifrach

Claim 23 provides (i) a frame buffer configured to pause a real-time frame during a transition from a real-time mode to a time-shifted mode, (ii) an encoder configured to generate and store a second signal, and (iii) a controller configured to present an output signal comprising the retrieved second signal when in a time-shifted mode. The Examiner has asserted that a normal viewing mode of Yifrach discloses the claimed real-time mode and a playback mode of Yifrach discloses the claimed time-shifted mode.[9] The text of Yifrach cited by the Examiner for the transition states:

> (c) Now whenever the viewer wishes to play back the 30 seconds of broadcast "frozen" by depressing the Freeze button 32, this is effected by depressing the Playback button 33, which controls the logic circuit 31 to select the Playback Mode.[10]

Nowhere in the above text or any other section does Yifrach disclose or suggest that real-time frames are **paused during a transition** from the real-time mode to the time-delayed mode as presently claimed. In contrast, Yifrach discloses that the "frozen" real-time frames used in the time-delay mode are **stored before a transition** from the real-time mode to the time-delay mode. In particular, Yifrach states:

> (b) When the Freeze button 32 is depressed, it controls the logic circuit 31 to select a Freeze Mode. In this mode, the cyclic storage device 23 is connected to the further storage device 30 to transfer its contents at that instant to the further storage device. That is, the last 30 seconds of the broadcast are thus "frozen" in the further storage device 30, while the cyclic storage device 23 continues to store the compressed audio and video signals last outputted by the compressor circuit 22 over the predetermined 30-second time interval.[11]

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[9] Advisory, April 7, 2003, page 2, lines 8-12.

[10] Yifrach, column 5, lines 12-16.

[11] Yifrach, column 4, line 64 to column 5, line 5.

Therefore, a transition from the normal viewing mode to the playback mode of Yifrach does not disclose or suggest pausing a real-time frame during a transition from a real-time mode to a time-shifted mode as presently claimed.

Assuming, *arguendo*, that a delayed viewing mode of Yifrach discloses the claimed time-shifted mode (for which the Appellant's representative does not necessarily agree), Yifrach is still silent regarding pausing a real-time frame during a transition between modes. Therefore, a transition from the normal viewing mode to the delayed viewing mode of Yifrach does not disclose or suggest pausing a real-time frame during a transition from a real-time mode and a time-delay mode as presently claimed.

Assuming, *arguendo*, that a freeze mode of Yifrach discloses the claimed time-shifted mode (for which the Appellant's representative does not necessarily agree), Yifrach is silent regarding a controller presenting an output signal comprising a retrieved signal (generated by an encoder) when in the time-shifted mode as presently claimed. In particular, the Examiner has asserted that a digitizer 21 of Yifrach discloses the claimed encoder and a logic block 26 of Yifrach discloses the claimed controller.[12] However, Yifrach is silent regarding the logic block 26 generating an output signal comprising a retrieved signal generated by the digitizer 21 when in the freeze mode. Therefore, Yifrach does not disclose or suggest an encoder configured to generate and store a second signal and a controller configured to present an output signal comprising the retrieved second signal when in a time-shifted mode as presently claimed.

Furthermore, claim 23 provides a structure comprising a frame buffer, an encoder, a buffer and a controller. The Examiner has asserted that a digitizer 21 of Yifrach discloses the

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[12] Office Action, December 31, 2002, page 3, lines 15-18.

claimed encoder, a cyclic storage device 23 of Yifrach discloses the claimed "buffer" (but does not distinguish the claimed frame buffer from the claimed buffer), and a logic block 26 of Yifrach discloses the claimed controller.[13] The **three elements** that the Examiner cites from Yifrach cannot anticipate the **four elements** from the claim. Yifrach is also silent regarding a frame buffer, a buffer and an encoder. Therefore, Yifrach does not disclose or suggest a structure comprising a frame buffer, an encoder, a buffer and a controller as presently claimed. Furthermore, the digitizer 21 (an analog to digital converter) of Yifrach is not an encoder. Therefore, Yifrach does not disclose or suggest an encoder as presently claimed.

In summary, Yifrach does not disclose or suggest pausing a real-time frame during a transition from a real-time mode to a time-shifted mode as presently claimed. Yifrach does not disclose or suggest a controller configured to present an output signal comprising the retrieved second signal when in a time-shifted mode as presently claimed. Yifrach also does not disclose or suggest a structure comprising a frame buffer, an encoder, a buffer and a controller as presently claimed. Furthermore, the digitizer 21 of Yifrach does not disclose or suggest a decoder as presently claimed. As such, the claimed invention is fully patentable over the cited reference and the rejection should be reversed.

B. Selected groupings of claims are each patentable over Yifrach

35 U.S.C. § 103

"[T]o establish obviousness based on a combination of the elements disclosed in the prior art, there must be some motivation, suggestion or teaching of the desirability of making the specific

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[13] Office Action, December 31, 2002, page 3, lines 17-18.

combination that was made by the applicants."[14] "[T]he factual inquiry whether to combine references must be thorough and searching."[15] "This factual question ... [cannot] be resolved on subjective belief and unknown authority."[16] "It must be based on objective evidence of record."[17] The Examiner must show that (a) there is some suggestion or motivation, either in the references or in the knowledge generally available to one of ordinary skill in the art, to modify or combine the references, (b) there is a reasonable expectation of success, and (c) the prior art reference (or combination of references) teaches or suggests all of the claim limitations as arranged in the claims.[18] Furthermore, The Court of Appeals for the Federal Circuit has indicated that the requirement for showing the teaching of motivation to combine references is "rigorous" and must be "clear and particular".[19]

1. Group 4 (claim 20) is fully patentable over Yifrach

Claim 20 provides a real-time decoder configured to pause a frame of a first output during a transition from a first mode to a second mode. The Examiner has admitted that Yifrach does not teach a real-time decoder, but has asserted that it would have been obvious to add a real-

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[14] *In re Kotzab*, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1316 (Fed. Cir. 2000) (citing *In re Dance*, 160 F.3d 1339, 1343, 48 USPQ2d 1635, 1637 (Fed. Cir. 1998); *In re Gordon*, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984)).

[15] *McGinley v. Franklin Sports, Inc.*, 262 F.3d 1339, 1351-52, 60 USPQ2d 1001, 1008 (Fed. Cir. 2001).

[16] *In re Lee*, 277 F.3d 1338, 1343-44, 61 USPQ2d 1430, 1434 (Fed. Cir. 2002).

[17] *Id.* at 1343, 61 USPQ2d at 1434.

[18] M.P.E.P. §2142.

[19] *In re Anita Dembiczak* and *Benson Zinbarg*, 50 U.S.P.Q.2d 1614 (Fed. Cir. 1999)

time decoder to Yifrach.[20] Assuming, *arguendo*, that adding a real-time decoder would have been obvious (for which the Appellant's representative does not necessarily agree), no evidence has been provided by the Examiner that the real-time decoder would be configured to pause a frame of a first output during a transition from a first mode to a second mode as presently claimed. Therefore, the Examiner has failed to establish *prima facie* obviousness due to missing claim limitations in the proposed combination.

Claim 20 further comprises (i) a frame storage system configured to store a compressed digital video signal and (ii) a time-shifted decoder coupled to the frame storage system and configured to generate a second output in response to the stored compressed digital video signal. The Examiner has admitted that Yifrach does not teach a frame storage system, but has asserted that it would have been obvious to add a frame storage system to Yifrach.[21] The Examiner has also asserted that the D/A converter 25 of Yifrach teaches the claimed time-shifted decoder.[22] Assuming, *arguendo*, that the proposed modification would have been obvious (for which the Appellant's representative does not necessarily agree), the proposed modification does not have a reasonable expectation of success. In particular, the frame storage system would store compressed digital video per the claim. However, the digital to analog converter 25 of Yifrach is not capable of decompressing the compressed digital video. Therefore, the Examiner has failed to establish a *prima facie* case for obviousness for lack of a reasonable expectation of success for the proposed modification.

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[20] Office Action, December 31, 2002, page 5, lines 3-10.

[21] Office Action, December 31, 2002, page 5, lines 3-4.

[22] Office Action, December 31, 2002, page 5, lines 4-6.

As stated above, the Examiner has also asserted that the D/A converter 25 of Yifrach teaches the claimed time-shifted decoder.[23] A digital to analog converter is not a decoder. Therefore, Yifrach does not teach or suggest a time-shifted decoder as presently claimed.

Furthermore, the proposed modification creates a conflict with the principle operation of Yifrach. All of the figures of Yifrach teach that the D/A converter 25 is coupled to a decompressor 24. If the D/A converter 25 is coupled to the decompressor 24, the proposed modified system does not teach or suggest the D/A converter 25 being coupled to the frame storage system. If the D/A converter 25 is coupled to the frame storage system instead of the decompressor 24, no mechanism would exist to convert a signal generated by the decompressor 24 into analog form for display on the screen 15. Thus, the proposed modification either (i) does not teach or suggest a time-shifted decoder coupled to a frame storage system as presently claimed or (ii) improperly changes the principle operation of the reference. The proposed modification cannot meet both the claim limitations and the normal operation of the reference simultaneously. Therefore, the Examiner has failed to establish *prima facie* obviousness due to a conflict between the proposed combination and the principle operation of the reference.

The Examiner has also failed to provide evidence of motivation to add a frame storage system to Yifrach. The Examiner has stated:

> It would have been further obvious to one having ordinary skill in the art at the time the invention was made to use a frame storage system that would store digital video signal separately from the real-time decoder in order to use it as a means for retrieving desirable frames at a later time, while making efficient use of the storage capacity.[24]

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[23] Office Action, December 31, 2002, page 5, lines 4-6.

[24] Office Action, December 31, 2002, page 5, lines 15-19.

In contrast, Yifrach already teaches a cyclic storage device 23 and a RAM 30 storing frames for retrieval at a later time.[25] No evidence has been provided by the Examiner why one of ordinary skill in the art would seek to add the storage capacity of the frame storage system above and beyond the storage capacity already present in Yifrach. No evidence has been provided by the Examiner that the frame storage system would make an efficient use of the storage capacity. The Examiner's comments appear to be merely conclusory statements and thus not evidence of motivation. The fact that the reference can be modified is not sufficient to establish obviousness.[26] Therefore, the Examiner has failed to establish *prima facie* obviousness for lack of evidence of motivation to make the proposed modifications.

In summary, the Examiner has failed to establish *prima facie* obviousness because the proposed modification (i) does not teach all of the claim limitations, (ii) does not have a reasonable expectation for success, (iii) either fails to create a claimed connection or changes the principle operation of the reference, (iv) lacks motivation to add the missing frame storage system and (v) does not teach or suggest a time-shifted decoder as presently claimed. As such, the claimed invention is fully patentable over the cited reference and the rejection should be reversed.

2. Group 5 (claims 21, 16 and 17) is fully patentable over Yifrach

Claim 21 provides a frame buffer configured to pause a frame of an output during a transition from a first mode to a second mode. The Examiner has admitted that Yifrach does not

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[25] Yifrach, FIGS. 1-4.

[26] Manual of Patent Examining Procedure (M.P.E.P.) Eighth Edition, Revised February 2003, §1243.01.

teach a frame buffer, but has asserted that it would have been obvious to add a frame buffer to Yifrach.[27] Assuming, *arguendo*, that adding a frame buffer would have been obvious (for which the Appellant's representative does not necessarily agree), no evidence has been provided by the Examiner that the frame buffer would be configured to pause a frame of an output during a transition from a first mode to a second mode as presently claimed. Therefore, the Examiner has failed to establish *prima facie* obviousness due to missing claim limitations in the proposed modification.

The Examiner has also asserted that the D/A converter 25 of Yifrach teaches the claimed time-shifted decoder.[28] A digital to analog converter is not a decoder. Therefore, Yifrach does not teach or suggest a time-shifted decoder as presently claimed.

Furthermore, the proposed modification creates a conflict with the principle operation of Yifrach. All of the figures of Yifrach teach that the D/A converter 25 receives a signal from a decompressor 24. If the D/A converter 25 receives the signal from the decompressor 24, the proposed modified system does not teach or suggest the D/A converter 25 operating in response to a stored uncompressed video signal from the frame storage system. If the D/A converter 25 responds to the uncompressed video signal stored in the frame storage system, no mechanism would exist to convert the signal generated by the decompressor 24 into analog form for display on the screen 15. Thus, the proposed modification either (i) does not teach or suggest a time-shifted decoder operating in response to a stored uncompressed video signal stored in a frame storage system as presently claimed or (ii) improperly changes the principle operation of the reference. The proposed modification cannot meet both the claim limitations and the normal operation of the reference

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[27] Office Action, December 31, 2002, page 5, line 21-page 6, line 2.

[28] Office Action, December 31, 2002, page 5, lines 4-6.

simultaneously. Therefore, the Examiner has failed to establish *prima facie* obviousness due to a conflict between the proposed combination and the principle operation of the reference.

The Examiner has also failed to provide evidence of motivation to add a frame storage system to Yifrach. The Examiner has stated:

> It would have been further obvious to one having ordinary skill in the art at the time the invention was made to use a frame storage system that would store digital video signal separately from the real-time decoder in order to use it as a means for retrieving desirable frames at a later time, while making efficient use of the storage capacity.[29]

In contrast, Yifrach already teaches a cyclic storage device 23 and a RAM 30 storing frames for retrieval at a later time.[30] No evidence has been provided by the Examiner why one of ordinary skill in the art would seek to add the storage capacity of the frame storage system above and beyond the storage capacity already present in Yifrach. No evidence has been provided by the Examiner that the frame storage system would make an efficient use of the storage capacity. The Examiner's comments appear to be merely conclusory statements and thus not not evidence of motivation. The fact that the reference can be modified is not sufficient to establish obviousness.[31] Therefore, the Examiner has failed to establish *prima facie* obviousness for lack of evidence of motivation to make the proposed modification.

In summary, the Examiner has failed to establish *prima facie* obviousness because the proposed modification (i) does not teach all of the claim limitations, (ii) either fails to create a claimed connection or changes the principle operation of the reference, (iii) lacks motivation to add

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[29] Office Action, December 31, 2002, page 5, lines 15-19.

[30] Yifrach, FIGS. 1-4.

[31] M.P.E.P., Eighth Edition, Revised February 2003, §1243.01.

the missing frame storage system and (iv) does not teach or suggest a time-shifted decoder as presently claimed. As such, the claimed invention is fully patentable over the cited reference and the rejection should be reversed.

3. Group 6 (claims 22, 13 and 14) is fully patentable over Yifrach

Claim 22 provides a controller configured to receive a compressed digital video input. The Examiner has stated that the rejection of claim 22 is based upon the same reasons for rejecting claims 20 and 21.[32] In particular, the Examiner has asserted that a logic block 26 of Yifrach teaches the claimed controller.[33] The Examiner has also asserted that Yifrach could be modified to operate in a digital broadcast environment.[34] However, Yifrach is silent regarding the logic block 26 receiving a compressed digital video input. In addition, the rational provided by the Examiner for rejecting claims 20 and 21 adds a real-time decoder without modifying the logic block 26 so that Yifrach could operate in conjunction with a digital broadcast environment. No assertion has been made by the Examiner that it would have been obvious to modify the logic block 26 of Yifrach to receive a compressed digital video input. No evidence of motivation has been provided by the Examiner to modify the logic block 26 of Yifrach to receive the compressed digital video input. Therefore, the proposed modification of Yifrach does not teach or suggest a controller configured to receive a compressed digital video input as presently claimed. The Examiner has also failed to

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[32] Office Action, December 31, 2002, page 6, lines 3-8.

[33] Office Action, December 31, 2002, page 5, lines 4-6.

[34] Office Action, December 31, 2002, page 5, lines 12-15.

establish *prima facie* obviousness for lack of evidence of motivation to modify the logic block 26 of Yifrach.

Claim 22 further provides a frame buffer configured to pause a frame of an output during a transition from a first mode to a second mode. The Examiner has admitted that Yifrach does not teach a frame buffer, but has asserted that it would have been obvious to add a frame buffer to Yifrach.[35] Assuming, *arguendo*, that adding a frame buffer would have been obvious (for which the Appellant's representative does not necessarily agree), no evidence has been provided by the Examiner that the frame buffer would be configured to pause a frame of an output during a transition from a first mode to a second mode as presently claimed. Therefore, the Examiner has failed to establish *prima facie* obviousness due to missing claim limitations in the proposed modification.

The Examiner has also asserted that the D/A converter 25 of Yifrach teaches the claimed time-shifted decoder.[36] A digital to analog converter is not a decoder. Therefore, Yifrach does not appear to teach or suggest a time-shifted decoder as presently claimed.

Furthermore, the proposed modification creates a conflict with the principle operation taught by Yifrach. All of the figures of Yifrach teach that the D/A converter 25 receives a signal from a decompressor 24. If the D/A converter 25 receives the signal from the decompressor 24, the proposed modification does not teach or suggest the D/A converter 25 operating in response to a stored uncompressed video signal from the frame storage system. If the D/A converter 25 responds to the uncompressed video signal stored in the frame storage system, no mechanism would exist to convert the signal generated by the decompressor 24 into analog form for display on the screen 15.

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[35] Office Action, December 31, 2002, page 5, line 21 to page 6, line 2.

[36] Office Action, December 31, 2002, page 5, lines 4-6.

Thus, the proposed modification either (i) does not teach or suggest a time-shifted decoder operating in response to a stored uncompressed video signal stored in a frame storage system as presently claimed or (ii) improperly changes the principle operation of the reference. The proposed modification cannot meet both the claim limitations and the normal operation of the reference simultaneously. Therefore, the Examiner has failed to establish *prima facie* obviousness due to a conflict between the proposed modification and the principle operation of the reference.

The Examiner has also failed to provide evidence of motivation to add a frame storage system to Yifrach. The Examiner has stated:

> It would have been further obvious to one having ordinary skill in the art at the time the invention was made to use a frame storage system that would store digital video signal separately from the real-time decoder in order to use it as a means for retrieving desirable frames at a later time, while making efficient use of the storage capacity.[37]

In contrast, Yifrach already teaches a cyclic storage device 23 and a RAM 30 storing frames for retrieval at a later time.[38] No evidence has been provided by the Examiner why one of ordinary skill in the art would seek to add the storage capacity of the frame storage system above and beyond the storage capacity already present in Yifrach. No evidence has been provided by the Examiner that the frame storage system would make an efficient use of the storage capacity. The Examiner's comments appear to be merely conclusory statements and thus not evidence of motivation. The fact that the reference can be modified is not sufficient to establish obviousness.[39] Therefore, the

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[37] Office Action, December 31, 2002, page 5, lines 15-19.

[38] Yifrach, FIGS. 1-4.

[39] M.P.E.P., Eighth Edition, Revised February 2003, §1243.01.

Examiner has failed to establish *prima facie* obviousness for lack of evidence of motivation to make the proposed modifications.

In summary, the Examiner has failed to establish *prima facie* obviousness because the proposed modification (i) does not teach all of the claim limitations for a frame buffer, (ii) either fails to create a claimed connection or changes the principle operation of the reference, (iii) lacks motivation to add the missing frame storage system, (iv) does not teach or suggest a time-shifted decoder as presently claimed and (v) does not teach all of the claim limitations for a controller as presently claimed. As such, the claimed invention is fully patentable over the cited reference and the rejection should be reversed.

C. Selected groupings of claims are each patentable over Yifrach in view of Russo et al.

35 U.S.C. § 103

"[T]o establish obviousness based on a combination of the elements disclosed in the prior art, there must be some motivation, suggestion or teaching of the desirability of making the specific combination that was made by the applicants."[40] "[T]he factual inquiry whether to combine references must be thorough and searching."[41] "This factual question ... [cannot] be resolved on

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[40] *In re Kotzab*, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1316 (Fed. Cir. 2000) (citing *In re Dance*, 160 F.3d 1339, 1343, 48 USPQ2d 1635, 1637 (Fed. Cir. 1998); *In re Gordon*, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984)).

[41] *McGinley v. Franklin Sports, Inc.*, 262 F.3d 1339, 1351-52, 60 USPQ2d 1001, 1008 (Fed. Cir. 2001).

subjective belief and unknown authority."[42] "It must be based on objective evidence of record."[43] The Examiner must show that (a) there is some suggestion or motivation, either in the references or in the knowledge generally available to one of ordinary skill in the art, to modify or combine the references, (b) there is a reasonable expectation of success, and (c) the prior art reference (or combination of references) teaches or suggests all of the claim limitations as arranged in the claims.[44] Furthermore, The Court of Appeals for the Federal Circuit has indicated that the requirement for showing the teaching of motivation to combine references is "rigorous" and must be "clear and particular".[45]

1. Group 7 (claim 11) is fully patentable over Yifrach in view of Russo et al.

The claim of group 7 depends from claim 1 and thus contains all of the limitations of claim 1. Consequently, the arguments presented above in support of the patentability of claim 1 (group 1) are incorporated hereunder in support of group 7.

Claim 11 provides that information is stored identifying a paused frame. Assuming, *arguendo*, that the proposed combination of Yifrach and Russo et al. would have been obvious (for which the Appellant's representative does not necessarily agree), the proposed combination still does not teach all of the limitations as presently claimed. In particular, Yifrach is silent regarding pausing real-time frames and Russo et al. do not cure the defect. Russo et al. teach that video programming

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[42] *In re Lee*, 277 F.3d 1338, 1343-44, 61 USPQ2d 1430, 1434 (Fed. Cir. 2002).

[43] *Id.* at 1343, 61 USPQ2d at 1434.

[44] M.P.E.P., §2142.

[45] *In re Anita Dembiczak* and *Benson Zinbarg*, 50 U.S.P.Q.2d 1614 (Fed. Cir. 1999)

material on a path 104 is written onto a disk 116 and then read from the disk 116 for presentation on a line 108 to a display device.[46] Any pause or mark information taught by Russo et al. identifies frames stored on the disk 116, not real-time frames on the line 104. Applying the teachings of Russo et al. to Yifrach would appear to provide a means to identify stored time-delayed frames in the cyclic storage device 23 of Yifrach but not paused real-time frames. Therefore, the proposed combination of Yifrach and Russo et al. does not teach or suggest that information is stored identifying a paused frame as presently claimed. As such, claim 11 is fully patentable over the cited references and the rejection should be reversed.

Groups 1-7 are separately patentable.

During prosecution, each independent and dependent claim is considered to be separately patentable over every other claim.[47] As such, each of the above groups is considered to be separately patentable over every other group.[48] In particular, each of the groups includes a unique combination of arguments that allow individual groups to stand over the references even if all of the other groups fall.

Group 1 includes an argument that Yifrach does not disclose or suggest pausing a real-time frame during a transition between modes.

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[46] Russo et al., FIG. 1 and column 4, lines 63-67.

[47] See, e.g., *Rowe v. Dror*, 42 USPQ2d 1550, 1552 (Fed. Cir. 1997), *Preemption Devices, Inc. v. Minnesota Mining and Manufacturing Company*, 221 USPQ 841, 843 (Fed. Cir. 1984), and *Jones v. Hardy*, 727 F.2d 1524, 1528, 220 USPQ 1021, 1024 (Fed. Cir. 1984) (It is well established that each claim in a patent constitutes a separate invention.).

[48] M.P.E.P., Eighth Edition, August, 2001, §1206.

Group 2 includes an argument that Yifrach does not disclose or suggest that the transition is between a paused frame and a time-delayed version of the paused frame. Since group 1 does not depend on the transition between specific frames argument, group 2 may be found patentable even if group 1 is not.

Group 3 includes an argument that Yifrach does not disclose or suggest a structure comprising a frame buffer, an encoder, a buffer and a controller. Since groups 1 and 2 do not depend on the structure argument, group 3 may be found patentable even if groups 1 and /or 2 are not.

Group 7 includes an argument that Yifrach and Russo et al. do not teach or suggest identifying a paused frame. Since groups 1-3 do not depend on the identifying argument, group 7 may be found patentable even if groups 1, 2 and/or 3 are not.

Group 4 includes an argument that Yifrach does not teach or suggest a frame storage system configured to store a compressed digital video signal. Since groups 1-3 and 7 do not depend on the frame storage system argument, group 4 may be found patentable even if groups 1, 2, 3 and/or 7 are not.

Group 5 includes an argument that a *prima facie* obvious case to add a frame buffer configured to pause a frame has not been established. Since groups 1-4 and 7 do not depend on the *prima facie* argument, group 5 may be found patentable even if groups 1, 2, 3, 4 and/or 7 are not.

Group 6 includes an argument that Yifrach does teach or suggest a controller configured to receive a compressed digital video input. Since groups 1-5 and 7 do not depend on the controller argument, group 6 may be found patentable even if groups 1, 2, 3, 4, 5 and/or 7 are not.

D. CONCLUSION

Yifrach does not disclose or suggest every claim limitation as arranged in claims 1-5 and 23. The proposed modifications of Yifrach (i) do not teach or suggest every claim limitation of claims 6-10, 13-22 and 24, (ii) do not have a reasonable expectation for success and/or (iii) conflict with the primary operation of the system of Yifrach. The proposed combination of Yifrach and Russo et al. does not teach or suggest identifying a paused frame per claim 11. Hence, the Examiner has clearly erred with respect to the patentability of the claimed invention. It is respectfully requested that the Board overturn the Examiner's rejection of all pending claims, and hold that the claims are not rendered anticipated or obvious by the cited references. However, should the Board find the arguments herein in support of independent claims 1, 20, 21, 22 and/or 23 unpersuasive, the Board is respectfully requested to carefully consider the arguments set forth above in support of each of the independently patentable groups.

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IX. APPENDIX

The claims of the present application which are involved in this appeal are as follows:

1. A time-shifted video method comprising:

in a real-time mode, delivering real-time video frames for display in response to a digital input signal,

in a time-shifted mode, delivering time-shifted video frames for display in response to a digital input signal, the time-shifted video frames being delayed relative to the real-time video frames, and

pausing a real-time frame during a transition from the real-time mode to the time-shifted mode.

2. The method of claim 1, wherein the transition is between the paused real-time frame and a time-shifted version of the paused real-time frame.

3. The method of claim 1, further comprising providing trick functions during the time-shifted mode.

4. The method of claim 1, wherein the transition mode is triggered by a command of a viewer or an event generated by software.

5. The method of claim 1, wherein the real-time video frames are derived from uncompressed video.

6. The method of claim 5, wherein the real-time video frames are provided from an input frame buffer.

7. The method of claim 1, wherein the real-time video frames are derived from input compressed video.

8. The method of claim 7, wherein the real-time frames are provided from a decoder that decompresses the input compressed video.

9. The method of claim 1, wherein the real-time mode, the time-shifted mode, and the transition are provided by a single codec chip.

10. The method of claim 8, wherein the compressed video comprises MPEG video.

11. The method of claim 1, wherein information is stored identifying the paused frame, and before the time-shifted mode occurs, a predetermined frame or a next frame after the predetermined frame is queued up.

13. The apparatus of claim 22, further comprising a real-time processing path including a real-time decoder and the time-shifted decoder that deliver real-time video to an output based on the digital video input.

14. The apparatus according to claim 13, wherein the real-time decoder and the time-shifted decoder are provided in a single codec.

15. The apparatus of claim 23, having a processing path for said real-time mode and a processing path for said time-shifted mode.

16. The apparatus of claim 21, wherein an encoder and the time-shifted decoder are provided in a single codec.

17. The apparatus of claim 21, wherein processing paths include buffers in a common memory.

18. The apparatus of claim 23, wherein the apparatus comprises a set-top box.

19. The apparatus of claim 23, wherein the apparatus is configured to present signals viewable by an analog television.

20. A set-top box comprising:

a real-time decoder configured to (i) generate a first output in response to a compressed digital video input signal and (ii) pause a frame of said first output during a transition from a first mode to a second mode,

a frame storage system configured to store said compressed digital video signal separately from said real-time decoder,

a time-shifted decoder (i) coupled to the frame storage system and (ii) configured to generate a second output in response to said stored compressed digital video signal, and

a controller configured to generate a command configured to control presenting (i) said first output when in said first mode and (ii) said second output when in said second mode, wherein said first output and said second output are viewable by a display device.

21. A television receiver comprising:

a frame buffer configured to (i) present an output in response to an uncompressed video signal and (ii) pause a frame of said output during a transition from a first mode to a second mode,

a frame storage system configured to store said uncompressed video signal separately from said frame buffer,

a time-shifted decoder configured to generate a second output in response to said stored uncompressed video signal, and

a controller configured to generate a command configured to control presenting (i) said first output when in said first mode and (ii) said second output when in said second mode, wherein said first output and said second output are viewable by a display device.

22. A set-top box comprising:

a controller configured to receive a command and a compressed digital video input,

a frame buffer configured to (i) generate a first output in response to the compressed digital video input and (ii) pause a frame of said first output during a transition from a first mode to a second mode,

a frame storage system coupled to the controller, and

a time-shifted decoder coupled to the frame storage system and the controller configured to generate a second output in response to (i) said compressed digital video input, and (ii) said command;

wherein the controller is configured to generate a second command configured to control presenting (i) said first output when in said first mode and (ii) said second output when in said second mode, wherein said first output and said second output are viewable by an analog display device.

23. An apparatus comprising:

a frame buffer configured to (i) generate a first signal in response to a digital input signal and (ii) pause a real-time frame during a transition from a real-time mode to a time-shifted mode;

an encoder configured to generate a second signal in response to said digital input signal, wherein said second signal is (i) stored in a buffer and (ii) retrieved separate from being stored; and

a controller configured to present an output signal comprising (i) said first signal when in said real-time mode and (ii) said retrieved second signal when in said time-shifted mode.

24. The method according to claim 2, wherein said transition is seamless to a viewer.